REMARKS

Claims 1, 4-9, 11-16, 18-22, 25-27, 33-34, 36-42, 44-48, and 50 are pending in the present application. In the Office Action dated May 26, 2005, claims 1, 2, 4-9, 11-17, 19-23, 25-27, 38-42, 44-48 and 50 were rejected under 35 U.S.C. 103(a) as being unpatentable over PCI System Architecture, Third Edition, by Tom Shanley, ("Shanley"), U.S. Patent No. 6,098,158 to Lay et al. ("Lay"), and Intel Application Note AP-758 'Flash Memory PCI Add-In Card for Embedded Systems' ("AP-758"). Claims 3, 10, 18, 24, 43, and 49 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shanley, AP-758, and Lay as applied to claims 2, 9, 17, 23, 39, and 46 above, and further in view of U.S. Patent No. 6,256,692 to Yoda et al. ("Yoda"). Claims 28-37 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shanley, Lay, AP-758, and Yoda.

The disclosed embodiments of the invention will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed embodiments include systems and methods for storing and restoring a machine state of a computer system. In this manner, relatively immediate operation of the computer system upon power-up can be made available, thereby avoiding the need to wait for the typical power-up sequence and boot routine to complete. One embodiment of a computer system includes a central processing unit (CPU) coupled to a memory via a local CPU bus, and further includes a PCI bus coupled to the first bus to provide communication with the CPU and the memory. The system also includes a PC card coupled to the PCI bus and a non-volatile memory for storing machine state information corresponding to the machine state. The PC card further includes a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom. The system may also include a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. In addition, a PCI-CardBus bridge is coupled to the PCI bus to provide communication between the PCI bus and the PC card coupled to the PCI-CardBus bridge. This allows the system to be used with easily removeable conventional PC cards so that the PC card may be moved from system to system to

transfer the machine state information. This is advantageous in terms of portability and ease of a system administrator (e.g., a human) to reboot the state of one machine on a completely different machine.

The cited references do not teach or suggest the above features of the embodiments, nor the desirability of the advantages that are derived therefrom, such as the ease of using a conventional PC card in combination with the other features of the embodiments to create a system that allows the user to easily move a machine state from one system to another. The Examiner has cited Shanley for disclosing the combination of a CPU coupled to a first bus and a memory connected to the first bus, and PC card coupled to a second bus and the CPU. The Examiner also cited Lay for teaching storing machine sate information in a non-volatile memory and a controller coupled to the non-voltaite memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system to improve boot up time. Thus, Lay is combined with Shanley in order to improve the boot up time of Shanley. AP758 is cited for disclosing a PC card coupled to a non-volatile memory for use in an embedded system. The Examiner has combined the teachings of Shanley, AP758, and Lay with the motivation for the combination primarily to create an embedded system, as disclosed in AP758, which employs the fast boot process of Lay.

The Examiner has also cited Yoda for the purposes of modifying the PC card disclosed in AP758 by providing a PCI-CardBus and replacing the large memory module of AP758 with a small business card sized PC card.

Applicants assert that there is no motivation from the cited references or knowledge commonly known in the art to employ a PCI-CardBus with AP758 so that the large memory module of AP758 can be replaced with a small business card sized PC card of Yoda. To the contrary, the cited references teach away from such a modification. Specifically, as combined by the Examiner, AP758 is combined with Lay and Shanley to create an embedded system. According to the Examiner, embedded systems are designed and used to function for long periods of time without human intervention. The large memory module of AP758 is clearly not designed nor intended to repeatedly removed and re-installed. Thus, there is no reason one of ordinary skill in the art would modify the disclosure of AP758, Lay, and Shanley with Yoda because the PCI-CardBus and PC card disclosed in Yoda is designed and intended to be used in a non-embedded system where the PC card is repeatedly removed and reinstalled. Again, such a system taught by Yoda is not embedded and certainly would not be used to function for long

periods of time without human intervention in contrast to the system of AP758. Therefore, manner in which Yoda is applied in combination with the other cited references is improper because the cited references clearly teach away from such a combination.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. As amended, claim 1 recites "a central processing unit (CPU); a local CPU bus coupled to the CPU; a memory coupled to the local CPU bus to store data accessible by the CPU via the local CPU bus; a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus; a PC card coupled to the PCI bus, the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system; and a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC card coupled to the PCI-CardBus bridge." (Emphasis Added) As discussed above, there is no motivation or suggestion in the cited references to create a computer system configured with the PC card coupled to a PCI-CardBus bridge so that small, portable, and easily removable PC cards may be used in the system to facilitate moving machine state information from one system to another. There is no motivation or suggestion to modify AP758 with Yoda because such a modification clearly teaches away from creating an embedded system, which was the basis for the combination of Lay, Shanley, and AP758. The manner in which Yoda is applied in combination with Lay, Shanley, and AP758 is the result of using impermissible hindsight to recreate the invention of claim 1 and not as a result of the teachings of the cited references.

As amended, claim 9 recite, in part, "a PC card coupled to the bus, the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system; and wherein the bus comprises a PCI bus, and the computer system further comprises a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC card coupled to the PCI-CardBus bridge." (Emphasis Added). Again, the cited references do not

provide the motivation or suggestion to provide such an interface in combination with the other claimed features, and claim 9 is patentable over the cited references for at least this reason.

As amended, claim 16 recites, in part, "a bus interface compatible with a CardBus and coupled to the PCI bus, the bus interface further coupled to the non-volatile memory and the controller to transfer data between the non volatile memory and the PCI bus in accordance with a data format and transfer protocol of the PCI bus." The cited references do not provide the motivation or suggestion to provide such an interface in combination with the other claimed features, and claim 16 is patentable over the cited references for at least this reason.

As amended, claim 22 recites, in part, "a CardBus compatible bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the non volatile memory and the PCI bus in accordance with a data format and transfer protocol of the PCI bus." Again, the cited references do not provide the motivation or suggestion to provide such an interface in combination with the other claimed features, and claim 22 is patentable over the cited references for at least this reason.

As amended, claim 33 recites, in part, "wherein the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the PCI bus in accordance with the PCI data format and transfer protocol." Again, the cited references do not provide the motivation or suggestion to provide such an interface in combination with the other claimed features, and claim 33 is patentable over the cited references for at least this reason.

As amended, claim 38 recites the acts "capturing the machine state of the computer system via a controller coupled to a non-volatile memory to control the storing of data therein and the retrieval of data therefrom; transferring machine state information corresponding to the captured machine state from the computer system to a PC card operably configured with the non-volatile memory; storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system; and wherein transferring the machine state information to the PC card comprises transferring data from the CPU and the memory to the PC card in accordance with a CardBus protocol. (Emphasis Added). The combination of the cited references does provide the motivation to perform the recited acts above and, in particular, transferring the machine state information to the PC card in accordance with a CardBus protocol.

As amended, claim 45 recites, in part, "wherein transferring the machine state information from the non-volatile memory comprises transferring data from PC card to the computer system in accordance with a CardBus protocol." Again, the combination of the cited references does provide the motivation to perform the recited acts above and, in particular, transferring the machine state information to the PC card in accordance with a CardBus protocol.

Claims depending from claims 1, 9, 16, 22, 33, 38, and 45 are also patentable due to depending from a patentable base claim and further in view of the additional limitations recited in the dependent claims.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
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